Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_

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**End Semester Examination – Nov/Dec – 2018**

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| **Code :** | **14EC2072** | **Duration :** | **3hrs** |
| **Sub. Name :** | **ANALYSIS AND DESIGN OF DIGITAL IC** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Sketch the physical structure of pMOS transistor and its schematic icon. | CO2 | 6 |
| b. | With neat diagram, illustrate the different regions of operation of NMOS transistor. | CO2 | 14 |
| (OR) | | | | |
| 2. | a. | Mention the value of Y in Fig 1a and 1b when A=0 and B=0. Justify the same.    Fig 1a Fig 1b | CO2 | 6 |
| b. | Define noise margin and analyse a CMOS structure with respect to its noise margin levels. | CO2 | 14 |
| 3. | a. | Justify the statement “NMOS transistors pass strong zero but not strong one”. | CO2 | 6 |
| b. | Analyze the voltage transfer curve of CMOS inverter and indicate the status of PMOS and NMOS transistors in different regions of operation. | CO2 | 14 |
| (OR) | | | | |
| 4. | a. | List the different capacitances in MOSFET transistor. | CO2 | 6 |
| b. | With suitable examples, distinguish between analytical delay model and empirical delay model. | CO2 | 14 |
|  |  |  |  |  |
| 5. | a. | Design a 2 input NAND gate using complementary CMOS and explain its operation. | CO1 | 6 |
| b. | Discuss the different types of power dissipation that occurs in CMOS inverter design. | CO3 | 14 |
| (OR) | | | | |
| 6. | a. | Design a 2 input XOR logic gate using transmission gate logic. | CO1 | 6 |
| b. | Illustrate the different issues that occur in dynamic logic design style and provide suitable solutions for the same. | CO3 | 14 |
|  |  |  |  |  |
| 7. | a. | Differentiate between foreground and background memory with suitable examples. | CO3 | 4 |
| b. | Design F=ABC using np-CMOS logic design style and explain its operation. | CO1 | 16 |
| (OR) | | | | |
| 8. | a. | Differentiate between combinational and sequential logic circuits with block diagram. | CO3 | 4 |
| b. | Explain the operation of clocked version of SR latch with respect to all input conditions of its characteristics table. | CO1 | 16 |
|  | |  |  |  |
|  | | **Compulsory**: |  |  |
| 9. | a. | Design a pipelined data path for the computation of log(la+bl) and explain its operation. | CO1 | 10 |
| b. | Design a 2 input OR gate using true single phase clocked approach and explain its operation. | CO1 | 10 |